ADC16061
Self-Calibrating 16-Bit, 2.5 MSPS, 390 mW A/D Converter

General Description
The ADC16061 is a self-calibrating 16-bit, 2.5 Megasample per second analog to digital converter. It operates on a single +5V supply, consuming just 390mW (typical).

The ADC16061 provides an easy and affordable upgrade from 12 bit and 14 bit converters. The ADC16061 may also be used to replace many hybrid converters with a resultant saving of space, power and cost.

The ADC16061 operates with excellent dynamic performance at input frequencies up to ½ the clock frequency. The calibration feature of the ADC16061 can be used to get more consistent and repeatable results over the entire operating temperature range. On-command self-calibration reduces many of the effects of temperature-induced drift, resulting in more repeatable conversions.

The Power Down feature reduces power consumption to less than 2mW.

The ADC16061 comes in a TQFP and is designed to operate over the commercial temperature range of 0°C to +70°C.

Features
- Single +5V Operation
- Self Calibration
- Power Down Mode

Key Specifications
- Resolution: 16 Bits
- Conversion Rate: 2.5 Msps (min)
- DNL: 1.0 LSB (typ)
- SNR (fIN = 500 kHz): 80 dB (typ)
- Supply Voltage: +5V ±5%
- Power Consumption: 390mW (typ)

Applications
- PC-Based Data Acquisition
- Document Scanners
- Digital Copiers
- Film Scanners
- Blood Analyzers
- Sonar/Radar

Connection Diagram

Ordering Information

<table>
<thead>
<tr>
<th>Commercial</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>(0°C ≤ T A ≤ +70°C)</td>
<td></td>
</tr>
<tr>
<td>ADC16061CCVT</td>
<td>VEG52A 52 Pin Thin Quad Flat Pack</td>
</tr>
<tr>
<td>ADC16061EVAL</td>
<td>Evaluation Board</td>
</tr>
</tbody>
</table>
Block Diagram

20-Stage Pipeline Converter

- \( V_{IN^+} \)
- \( V_{IN^-} \)
- \( V_{REF^+} \) OUT
- \( V_{REF^-} \) OUT
- \( V_{GAIN} \) Coef.
- \( V_{CM} \) to internal circuitry
- \( V_{REF^+} \) OUT
- \( V_{REF^-} \) OUT
- \( V_{REF} \) (MID)
- \( V_{REF} \) OUT

Clock
Reset
CAL
\( \bar{R}D \)
\( \bar{R}O \)

Sequencer
ALU
Correction
RAW

Output Buffers

16

16

D00-D15

EOC
<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Equivalent Circuit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog I/O</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>$V_{\text{IN}^+}$</td>
<td><img src="image1" alt="Equivalent Circuit" /></td>
<td>Non-Inverting analog signal input. With a 2.0V reference voltage and a 2.0V common mode voltage, $V_{\text{CM}}$, the input signal voltage range is from 1.0 volt to 3.0 Volts.</td>
</tr>
<tr>
<td>4</td>
<td>$V_{\text{IN}^-}$</td>
<td><img src="image2" alt="Equivalent Circuit" /></td>
<td>Inverting analog signal input. With a 2.0V reference voltage and a 2.0V common mode voltage, $V_{\text{CM}}$, the input signal voltage range is from 1.0 Volt to 3.0 Volts. The input signal should be balanced for best performance.</td>
</tr>
<tr>
<td>48</td>
<td>$V_{\text{REF}^+ \text{ in}}$</td>
<td><img src="image3" alt="Equivalent Circuit" /></td>
<td>Positive reference input. This pin should be bypassed to AGND with a 0.1 $\mu$F monolithic capacitor. $V_{\text{REF}^+}$ minus $V_{\text{REF}^- \text{ in}}$ should be a minimum of 1.8V and a maximum of 2.2V. The full-scale input voltage is equal to $V_{\text{REF}^+ \text{ in}}$ minus $V_{\text{REF}^- \text{ in}}$.</td>
</tr>
<tr>
<td>47</td>
<td>$V_{\text{REF}^- \text{ in}}$</td>
<td><img src="image4" alt="Equivalent Circuit" /></td>
<td>Negative reference input. In most applications this pin should be connected to AGND and the full reference voltage applied to $V_{\text{REF}^+ \text{ in}}$. If the application requires that $V_{\text{REF}^- \text{ in}}$ be offset from AGND, this pin should be bypassed to AGND with a 0.1 $\mu$F monolithic capacitor. The full-scale input voltage is equal to $V_{\text{REF}^+ \text{ in}}$ minus $V_{\text{REF}^- \text{ in}}$.</td>
</tr>
<tr>
<td>50</td>
<td>$V_{\text{REF}^+ \text{ out}}$</td>
<td><img src="image5" alt="Equivalent Circuit" /></td>
<td>Output of the high impedance positive reference buffer. This pin should be bypassed to AGND with a 0.1 $\mu$F monolithic capacitor in parallel with a 10 $\mu$F capacitor.</td>
</tr>
<tr>
<td>49</td>
<td>$V_{\text{REF}^- \text{ out}}$</td>
<td><img src="image6" alt="Equivalent Circuit" /></td>
<td>The output of the negative reference buffer. This pin should be bypassed to AGND with a 0.1 $\mu$F monolithic capacitor in parallel with a 10 $\mu$F capacitor.</td>
</tr>
<tr>
<td>52</td>
<td>$V_{\text{REF (MID)}}$</td>
<td><img src="image7" alt="Equivalent Circuit" /></td>
<td>Output of the reference mid-point. This pin should be bypassed to AGND with a 0.1 $\mu$F monolithic capacitor. This voltage is derived from $V_{\text{CM}}$.</td>
</tr>
<tr>
<td>51</td>
<td>$V_{\text{CM}}$</td>
<td><img src="image8" alt="Equivalent Circuit" /></td>
<td>Input to the common mode buffer, nominally equal to 40% of the supply voltage (2.0V). This pin should be bypassed to AGND with a 0.1 $\mu$F monolithic capacitor. Best performance is obtained if this pin is driven with a low impedance source of 2.0V.</td>
</tr>
</tbody>
</table>
## Pin Descriptions and Equivalent Circuits

### Digital I/O

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Equivalent Circuit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>CLOCK</td>
<td><img src="image1" alt="CLOCK Equivalent Circuit" /></td>
<td>Digital clock input. The input voltage is captured ( t_{AD} ) after the fall of the clock signal. The clock frequency should not be changed or interrupted during conversion or while reading data output.</td>
</tr>
<tr>
<td>11</td>
<td>CAL</td>
<td><img src="image2" alt="CAL Equivalent Circuit" /></td>
<td>CAL is a level-sensitive digital input that, when pulsed high for at least two clock cycles, puts the ADC into the CALIBRATE mode. See Section 2.3.</td>
</tr>
<tr>
<td>40</td>
<td>RESET</td>
<td><img src="image3" alt="RESET Equivalent Circuit" /></td>
<td>RESET is a level-sensitive digital input that, when pulsed high for at least 2 CLOCK cycles, results in the resetting of the ADC. This reset pulse must be applied after ADC power-up, before calibration.</td>
</tr>
<tr>
<td>18</td>
<td>RD</td>
<td><img src="image4" alt="RD Equivalent Circuit" /></td>
<td>RD is the (READ) digital input that, when low, enables the output data buffers. When this input pin is high, the output data bus is in a high impedance state.</td>
</tr>
<tr>
<td>44</td>
<td>PD</td>
<td><img src="image5" alt="PD Equivalent Circuit" /></td>
<td>PD is the Power Down input that, when low, puts the converter into the power down mode. When this pin is high, the converter is in the active mode.</td>
</tr>
<tr>
<td>17</td>
<td>EOC</td>
<td><img src="image6" alt="EOC Equivalent Circuit" /></td>
<td>EOC is a digital output that, when low, indicates the availability of new conversion results at the data output pins.</td>
</tr>
<tr>
<td>21-32</td>
<td>D00-15</td>
<td><img src="image7" alt="D00-15 Equivalent Circuit" /></td>
<td>Digital data outputs that make up the 16-bit TRI-STATE conversion results. D00 is the LSB, while D15 is the MSB (SIGN bit) of the two’s complement output word.</td>
</tr>
</tbody>
</table>

### Analog Power

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6, 7, 45</td>
<td>VA</td>
<td>Positive analog supply pins. These pins should be connected to a clean, quiet +5V source and bypassed to AGND with 0.1 μF monolithic capacitors in parallel with 10 μF capacitors, both located within 1 cm of these power pins.</td>
</tr>
<tr>
<td>5, 8, 46</td>
<td>AGND</td>
<td>The ground return for the analog supply. AGND and DGND should be connected together directly beneath the ADC16061 package. See Section 5 (Layout and grounding) for more details.</td>
</tr>
</tbody>
</table>

### Digital Power

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>VD</td>
<td>Positive digital supply pin. This pin should be connected to the same clean, quiet +5V source as is VA and bypassed to DGND with a 0.1 μF monolithic capacitor in parallel with a 10μF capacitor, both located within 1 cm of the power pin.</td>
</tr>
<tr>
<td>12, 13, 14, 19, 41, 42, 43</td>
<td>DGND</td>
<td>The ground return for the digital supply. AGND and DGND should be connected together directly beneath the ADC16061 package. See Section 5 (Layout and Grounding) for more details.</td>
</tr>
<tr>
<td>Pin No.</td>
<td>Symbol</td>
<td>Equivalent Circuit</td>
</tr>
<tr>
<td>---------</td>
<td>--------</td>
<td>---------------------</td>
</tr>
<tr>
<td>34</td>
<td>V_D I/O</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>DGND I/O</td>
<td></td>
</tr>
<tr>
<td>NC</td>
<td>NC</td>
<td></td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

- Supply Voltage \((V_A, V_D, V_D \text{ I/O})\) 6.5V
- Voltage on Any I/O Pin −0.3V to \((V_A +0.3V)\)
- Input Current at Any Pin (Note 3) ±25mA
- Package Input Current (Note 3) ±50mA
- Power Dissipation at \(T_A = 25^\circ C\) (Note 4)
- ESD Susceptibility (Note 5)
  - Human Body Model 1500V
  - Machine Model 200V
- Soldering Temp., Infrared, 10 sec. (Note 6) 300˚C
- Storage Temperature −65˚C to +150˚C

Operating Ratings (Notes 1, 2)

- Operating Temperature \(0^\circ C \leq T_A \leq +70^\circ C\)
- Range
  - \(V_A, V_D\) +4.75V to +5.25V
  - \(V_D \text{ I/O}\) 2.7V to \(V_D\)
  - \(V_{\text{REF} - \text{IN}}\) 1.0V to 3.0V
  - \(V_{\text{REF} - \text{IN}}\) AGND to 1.0V
- Digital Inputs −0.05V to \(V_D + 0.05V\)
- \(| V_A - V_D | \leq 100 \text{ mV}\)
- \(| AGND - DGND | \leq 100 \text{ mV}\)

Package Thermal Resistance

<table>
<thead>
<tr>
<th>Package</th>
<th>(\theta_{JA})</th>
</tr>
</thead>
<tbody>
<tr>
<td>32-Lead TQFP</td>
<td>70˚C / W</td>
</tr>
</tbody>
</table>

Converter Electrical Characteristics

The following specifications apply for AGND = DGND = DGND \(\text{ I/O = 0V, } V^+ = V_A = V_D = +5.0V, V_D \text{ I/O = 3.0V or 5.0V, }\)
\(PD = +5V, V_{\text{REF}+ \text{ IN}} = +2.0V, V_{\text{REF} - \text{IN}} = \text{ AGND, } f_{\text{CLK}} = 2.5 \text{ MHz, } C_L = 50 \text{ pF/pin. After Auto-Cal.} \)

**Boldface limits apply for \(T_A = T_J = T_{\text{MIN}} \text{ to } T_{\text{MAX}}\):** all other limits \(T_A = T_J = 25^\circ C \) (Notes 7, 8, 9)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typical (Note 10) Limits (Note 11)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{\text{IN}}</td>
<td>Input Voltage Range ((V_{\text{IN}+} - V_{\text{IN}-}))</td>
<td>2.0</td>
<td>1.8</td>
<td>2.2</td>
</tr>
<tr>
<td>C_{\text{IN}}</td>
<td>Input Capacitance</td>
<td>(V_{\text{IN}} = 1.0V + 0.7V_{\text{rms}}) (CLK LOW)</td>
<td>12</td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(CLK HIGH)</td>
<td>28</td>
<td>pF</td>
</tr>
<tr>
<td>V_{\text{REF}}</td>
<td>Reference Voltage Range ([V_{\text{REF}+ \text{ IN}} - (V_{\text{REF} - \text{IN}})]) (Note 14)</td>
<td>2.00</td>
<td>1.8</td>
<td>V (min)</td>
</tr>
<tr>
<td></td>
<td>Reference Input Resistance</td>
<td></td>
<td>2.2</td>
<td>V (max)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Static Converter Characteristics**

- Resolution with No Missing Codes 15 Bits (min)
- INL Integral Non Linearity At 16 Bits ±3 ±9 LSB (max)
- DNL Differential Non Linearity At 16 Bits ±1 +3 ±2 LSB (min)
- Full-Scale Error ±0.6 ±3 % FS (max)
- Zero Error +0.1 ±0.7 % FS (max)

Reference and Analog Input Characteristics

- VIN Input Voltage Range \((V_{\text{IN}+} - V_{\text{IN}-})\)
- C_{\text{IN}} Input Capacitance
- V_{\text{REF}} Reference Voltage Range \([V_{\text{REF}+ \text{ IN}} - (V_{\text{REF} - \text{IN}})]\) (Note 14)
- Reference Input Resistance

Dynamic Converter Characteristics

- BW Full Power Bandwidth
- SNR Signal-to-Noise Ratio
- SINAD Signal-to-Noise & Distortion
- THD Total Harmonic Distortion
- SFDR Spurious Free Dynamic Range
- IMD Intermodulation Distortion

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## DC and Logic Electrical Characteristics

The following specifications apply for AGND = DGND = DGND I/O = 0V, V+ = V_A = V_D = +5.0V, VD I/O = 3.0V or 5.0V, PD = +5V, VREF+ = +2.0V, VREF IN = AGND, fCLK = 2.5 MHz, RS = 25Ω, C_L = 50 pF/pin. After Auto-Cal. **Boldface limits apply for TA = TJ = T_MIN to T_MAX:** all other limits TA = TJ = 25˚C (Notes 7, 8, 9)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typical (Note 10)</th>
<th>Limits (Note 11)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CLOCK, RD, PD Digital Input Characteristics</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{IN(1)}</td>
<td>Logical &quot;1&quot; Input Voltage</td>
<td>V+ = 5.25V</td>
<td>2.0</td>
<td>V (min)</td>
<td></td>
</tr>
<tr>
<td>V_{IN(0)}</td>
<td>Logical &quot;0&quot; Input Voltage</td>
<td>V+ = 4.75V</td>
<td>0.8</td>
<td>V (max)</td>
<td></td>
</tr>
<tr>
<td>I_{IN(1)}</td>
<td>Logical &quot;1&quot; Input Current</td>
<td>V_IN = 5.0V</td>
<td>5</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>I_{IN(0)}</td>
<td>Logical &quot;0&quot; Input Current</td>
<td>V_IN = 0V</td>
<td>−5</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>C_{IN}</td>
<td>V_IN Input Capacitance</td>
<td></td>
<td>5</td>
<td>pF</td>
<td></td>
</tr>
</tbody>
</table>

| **CAL, RESET Digital Input Characteristics** | | | | | |
| V_{IN(1)} | Logical "1" Input Voltage | V+ = 5.25V | 3.5 | V (min) |
| V_{IN(0)} | Logical "0" Input Voltage | V+ = 4.75V | 1.0 | V (max) |
| I_{IN(1)} | Logical "1" Input Current | V_IN = 5.0V | 5 | μA |
| I_{IN(0)} | Logical "0" Input Current | V_IN = 0V | −5 | μA |
| C_{IN} | Input Capacitance | | 5 | pF |

| **D00 - D13 Digital Output Characteristics** | | | | | |
| V_{OUT(1)} | Logical "1" Output Voltage | V_D I/O = 4.75V, I_{OUT} = −360 μA | 4.5 | V (min) |
| V_{OUT(1)} | Logical "1" Output Voltage | V_D I/O = 2.7V, I_{OUT} = −360 μA | 2.5 | V (min) |
| V_{OUT(0)} | Logical "0" Output Voltage | V_D I/O = 5.25V, I_{OUT} = 1.6 mA | 0.4 | V (max) |
| V_{OUT(0)} | Logical "0" Output Voltage | V_D I/O = 3.3V, I_{OUT} = 1.6 mA | 0.4 | V (max) |
| I_{OZ} | TRI-STATE Output Current | V_OUT = 3V or 5V | 100 | nA |
| I_{OZ} | TRI-STATE Output Current | V_OUT = 0V | −100 | nA |
| +I_{SC} | Output Short Circuit Source Current | V_OUT = 0V, V_D I/O = 3V | −10 | mA |
| −I_{SC} | Output Short Circuit Sink Current | V_OUT = V_D I/O = 3V | 12 | mA |

| **Power Supply Characteristics** | | | | | |
| I_A | Analog Supply Current | PD = V_D I/O | 70 | 85 | mA (max) |
| I_D | Digital Supply Current | PD = V_D I/O | 7 | 8 | mA (max) |
| I_D I/O | Output Bus Supply Current | PD = V_D I/O | 1 | 2 | mA (max) |
| | Total Power Consumption | PD = V_D I/O | 390 | 475 | mW (max) |
| | PD = DGND | | <2 | | mW |
| PSRR | Power Supply Rejection Ratio | Change in Full Scale as V_A goes from 4.25V to 5.25V | 68 | | dB |
| | 250 mV_P-P, 10 MHz riding on V_A | | 54 | | dB |

## AC Electrical Characteristics

The following specifications apply for AGND = DGND = DGND I/O = 0V, V+ = V_A = V_D = +5.0V, VD I/O = 3.0V or 5.0V, PD = +5V, VREF+ = +2.0V, VREF IN = AGND, fCLK = 2.5 MHz, RS = 25Ω, C_L = 50 pF/pin. After Auto-Cal. **Boldface limits apply for TA = TJ = T_MIN to T_MAX:** all other limits TA = TJ = 25˚C (Notes 7, 8, 9)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typical (Note 10)</th>
<th>Limits (Note 11)</th>
<th>Units (Limits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>f_{CLK}</td>
<td>Conversion Clock (CLOCK) Frequency</td>
<td></td>
<td>300</td>
<td>3</td>
<td>kHz (min)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.5</td>
<td>kHz (max)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Conversion Clock Duty Cycle</td>
<td></td>
<td>45</td>
<td>55</td>
<td>% (min)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>% (max)</td>
</tr>
<tr>
<td>t_{CONV}</td>
<td>Conversion Latency</td>
<td></td>
<td>13</td>
<td></td>
<td>Clock Cycles</td>
</tr>
</tbody>
</table>
AC Electrical Characteristics (Continued)

The following specifications apply for AGND = DGND = DGND I/O = 0V, V+ = VA = VD = +5.0V, VD I/O = 3.0V or 5.0V, PD = +5V, VREF+ = +2.0V, VREF IN = AGND, fCLK = 2.5 MHz, RS = 25Ω, C L = 50 pF/pin. After Auto-Cal. Boldface limits apply for TA = TJ = TMIN to TMAX: all other limits TA = TJ = 25˚C (Notes 7, 8, 9)

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</tr>
</thead>
<tbody>
<tr>
<td>tAD</td>
<td>Aperture Delay</td>
<td>9</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tOD</td>
<td>Falling edge of CLK to Data Valid</td>
<td>50</td>
<td>38</td>
<td>ns (min)</td>
<td>95</td>
</tr>
<tr>
<td>tEOCL</td>
<td>Falling edge of CLK to falling edge of EOC</td>
<td>1/(4fCLK)</td>
<td>90</td>
<td>ns (min)</td>
<td>130</td>
</tr>
<tr>
<td>tON</td>
<td>RD low to data valid on D00 -D15</td>
<td>23</td>
<td>33</td>
<td>ns (max)</td>
<td></td>
</tr>
<tr>
<td>tOFF</td>
<td>RD high to D00 -D15 in TRI-STATE</td>
<td>25</td>
<td>33</td>
<td>ns (max)</td>
<td></td>
</tr>
<tr>
<td>tCAL</td>
<td>Calibration Time</td>
<td>110</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND = AGND = DGND I/O = 0V, unless otherwise specified.

Note 3: When the input voltage at any pin exceeds the power supplies (that is, VIN < AGND or VIN > VA or VD), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current ratings limit the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

Note 4: The absolute maximum junction temperature (TJMAX) for this device is 150˚C. The maximum allowable power dissipation is dictated by TJMAX, the junction-to-ambient thermal resistance (θJA), and the ambient temperature (TA), and can be calculated using the formula PDMAX = (TJMAX - TA)/θJA. The values for maximum power dissipation will be reached only when the ADC16061 is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

Note 5: Human body model is 100 pF capacitor discharged through a 1.5kΩ resistor. Machine model is 220 pF discharged through ZERO Ω.

Note 6: See AN450, “Surface Mounting Methods and Their Effect on Product Reliability”, or the section entitled “Surface Mount” found in any post 1986 National Semiconductor Linear Data Book, for other methods of soldering surface mount devices.

Note 7: The inputs are protected as shown below. Input voltages above VA or below GND will not damage this device, provided current is limited per Note 3. However, errors in the A/D conversion can occur if the input goes above VA or below GND by more than 100 mV. As an example, if VA is 4.75 VDC, the full-scale input voltage must be ≤ 4.85 VDC to ensure accurate conversions.

Note 8: To guarantee accuracy, it is required that VA and VD be connected together and to the same power supply with separate bypass capacitors at each V+ pin.

Note 9: With the test condition for VREF = (VREF+ - VREF-) given as +2.0V, the 16-bit LSB is 30 µV.

Note 10: Typical figures are at TA = TJ = 25˚C, and represent most likely parametric norms.

Note 11: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level) with 50% duty cycle clock.

Note 12: Integral Non Linearity is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full-scale and negative full-scale.

Note 13: Timing specifications are tested at the TTL logic levels, VIN = 0.4V for a falling edge and VIN = 2.4V for a rising edge. TRI-STATE output voltage is forced to 1.4V.

Note 14: Optimum SNR performance will be obtained by keeping the reference voltage in the 1.8V to 2.2V range. The LM4041CIM3-ADJ (SOT-23 package), or the LM4041CIZ-ADJ (TO-92 package), bandgap voltage reference is recommended for this application.
**Electrical Characteristics (continued)**

**FIGURE 1. Transfer Characteristics**

\[ V_{IN} \text{ WHERE } V_{IN}^+ < V_{IN}^- \]

\[ 0111,1111,1111,1111 (+8191) \]
\[ 0111,1111,1111,1110 (+8190) \]

**NEGATIVE FULL-SCALE TRANSITION**

**ZERO TRANSITION**

\[ V_{IN} \text{ WHERE } V_{IN}^+ > V_{IN}^- \]

\[ 1000,0000,0000,00001 (-32767) \]
\[ 1000,0000,0000,0000 (-32768) \]

**ANALOG INPUT VOLTAGE**

\[ V_{IN} = (V_{IN}^+ - V_{IN}^-) \]

**FIGURE 2. Errors removed by Auto-Cal cycle**

**NEGATIVE FULL-SCALE ERROR**

**POSITIVE FULL-SCALE ERROR**

**ZERO ERROR**

\[ V_{IN} \text{ WHERE } V_{IN}^+ < V_{IN}^- \]

\[ +32767 \]

\[ -0.5 \text{ LSBs} \]
\[ -1.0 \text{ LSBs} \]
\[ -1.5 \text{ LSBs} \]

**NEGATIVE LINEARITY ERROR**

**POSITIVE LINEARITY ERROR**

\[ V_{IN} \text{ WHERE } V_{IN}^+ > V_{IN}^- \]

\[ (\text{from } -32768 \text{ to } +32767) \]
Typical Performance Characteristics

**INL**

![INL vs. Temperature](image)

**DNL**

![DNL vs. Temperature](image)

**SNR vs. Temperature**

![SNR vs. Temperature](image)

**INL vs. V_REF and Temperature**

![INL vs. V_REF and Temperature](image)
Typical Performance Characteristics

DNL vs. V_{REF}

\[ f_{CLK} = 2.5 \text{ MHz} \]
\[ f_{IN} = 500 \text{ kHz} \]
Temp. = -45°C to 85°C

[Graph showing DNL vs. V_{REF}]

SINAD & ENOB vs. Temperature

\[ V_A = 4.75V \text{ to } 5.25V \]
\[ f_{CLK} = 2.5 \text{ MHz} \]
\[ f_{IN} = 500 \text{ kHz} \]

[Graph showing SINAD & ENOB vs. Temperature]

SFDR vs. Temperature

\[ V_A = 4.75V \]
\[ f_{IN} = 500 \text{ kHz} \]
\[ V_A = 5.0V \]
\[ V_A = 5.25V \]

[Graph showing SFDR vs. Temperature]

THD vs. Temperature

\[ f_{CLK} = 2.5 \text{ MHz} \]
\[ f_{IN} = 500 \text{ kHz} \]
\[ V_A = 4.75V \]
\[ V_A = 5.0V \]
\[ V_A = 5.25V \]

[Graph showing THD vs. Temperature]

SINAD & ENOB vs. Clock Duty Cycle

55% Duty
50% Duty
40% Duty
60% Duty
45% Duty

[Graph showing SINAD & ENOB vs. Clock Duty Cycle]

IMD

[Graph showing IMD]
Typical Performance Characteristics  (Continued)

Specification Definitions

APERTURE DELAY is the time required after the falling edge of the clock for the sampling switch to open. The Track/Hold circuit effectively stops capturing the input signal and goes into the "hold" mode \( t_{AD} \) after the fall of the clock. APERTURE JITTER is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as \( \frac{\text{SINAD} - 1.76}{6.02} \) and says that the converter is equivalent to an ideal ADC of this (ENOB) number of bits.

FULL SCALE ERROR is the difference between the input voltage \( (V_{IN+} - V_{IN-}) \) just causing a transition to positive full scale and \( V_{REF} - 1.5 \text{ LSB} \), where \( V_{REF} \) is \( (V_{REF+}) - (V_{REF-}) \).

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the first and second order intermodulation products to the total power in one of the original frequencies. IMD is usually expressed in dB.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (\( \frac{1}{2} \text{ LSB} \) below the first code transition) through positive full scale (the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

MISSING CODES are those output codes that are skipped and will never appear at the ADC outputs. These codes can not be reached by any input value.

OUTPUT DELAY is the time delay after the falling edge of the input clock before the data update is present at the output pins.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is presented to the output stage. Data for any given sample is available the Pipeline Delay plus the Output Delay after that sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well an a.c. signal riding upon the power supply is rejected at the output. PSRR is measured with 10MHz, 250mV\(_{P-P}\) riding upon the power supply and is the ratio of the output amplitude of that signal to its amplitude on the power supply. PSRR is expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms value of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB or dBc, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics, but excluding d.c.

ZERO ERROR is the difference between the ideal differential input voltage (\( \frac{1}{2} \text{ LSB} \)) and the actual input voltage that just causes an transition from an output code of 32767 to an output code of 32768.
Timing Diagrams

TIMING DIAGRAM 1. Output Timing

Minimum $f_{CLK}$ is 300 kHz

TIMING DIAGRAM 2. Reset and Calibration Timing

Note: Minimum $f_{CLK}$ is 300 kHz
Functional Description

Operating on a single +5V supply, the ADC16061 uses a pipeline architecture and has error correction circuitry and a calibration mode to help ensure maximum performance at all times.

Balanced analog signals with a peak-to-peak voltage equal to the input reference voltage, $V_{REF}$, and centered around the common mode input voltage, $V_{CM}$, are digitized to 16 bits (15 bits plus sign). Neglecting offsets, positive input signal voltages ($V_{IN+} - V_{IN-} \geq 0$) produce positive digital output data and negative input signal voltages ($V_{IN+} - V_{IN-} < 0$) produce negative output data. The input signal can be digitized at any clock rate between 300 Ksps and 2.5 Msps.

Input voltages below the negative full scale value will cause the output word to take on the negative full scale value of $1000\ldots1111\ldots1111$. Input voltage above the positive full scale value will cause the output word to take on the positive full scale value of $0111\ldots1111\ldots1111$.

The output word rate is the same as the clock frequency. The analog input voltage is acquired at the falling edge of the clock and the digital data for that sample is delayed by the pipeline for 13 clock cycles plus $t_{DATA\_VALID}$. The digital output is undefined if the chip is being reset or is in the calibration mode. The output signal may be inhibited by the RD pin while the converter is in one of these modes.

The RD pin must be low to enable the digital outputs. A logic low on the power down (PD) pin reduces the converter power consumption to less than two milliwatts.

Applications Information

1.0 OPERATING CONDITIONS

We recommend that the following conditions be observed for operation of the ADC16061:

- $4.75\text{V} \leq V_A \leq 5.25\text{V}$
- $5.25\text{V} \leq V_D \leq 5.25\text{V}$
- $3.0\text{V} \leq V_{DI/O} \leq V_D$
- $0.3\text{MHz} \leq f_{CLK} \leq 2.5\text{ MHz}$
- $V_{CM} = 2.0\text{V}$
- $V_{REF\_IN+} = 2.0\text{V}$
- $V_{REF\_IN-} = AGND$

1.1 The Analog Inputs

The ADC16061 has two analog signal inputs, $V_{IN+}$ and $V_{IN-}$. These two pins form a balanced input. There are two reference pins, $V_{REF\_IN+}$ and $V_{REF\_IN-}$. These pins form a differential input reference.

1.2 Reference Inputs

$V_{REF\_IN+}$ should always be more positive than $V_{REF\_IN-}$. The effective reference voltage, $V_{REF}$, is the difference between these two voltages:

$$V_{REF} = (V_{REF\_IN+}) - (V_{REF\_IN-}).$$

The operational voltage range of $V_{REF\_IN+}$ is +1.8 Volts to +3.0 Volts. The operational voltage range of $V_{REF\_IN-}$ is ground to 1.0V. For best performance, the difference between $V_{REF\_IN+}$ and $V_{REF\_IN-}$ should remain within the range of 1.8V to 2.2V. Reducing the reference voltage below 1.8V will decrease the signal-to-noise ratio (SNR) of the ADC16061. Increasing the reference voltage (and, consequently, the input signal swing) above 2.2V will increase THD.

$V_{CM}$, the input common mode voltage, is set with on-board resistors to be 40% of the $V_A$ supply voltage. This pin should be bypassed to AGND with a 0.05µF to 0.1µF capacitor. Alternatively, drive this pin to a stable 2.0V with a low impedance source.

$V_{REF\_OUT\_IN+}$ and $V_{REF\_OUT\_IN-}$ and $V_{REF\_OUT\_MID}$ are the reference buffer outputs. The voltage at $V_{REF\_OUT\_MID}$ is nominally equal to $V_{CM}$ (2.0V), while the voltages at $V_{REF\_OUT\_IN+}$ and $V_{REF\_OUT\_IN-}$ are $V_{REF}$ above and below below $V_{CM}$ such that

$$V_{REF\_OUT\_IN+} = V_{CM} + \frac{1}{2}V_{REF}.$$  $$V_{REF\_OUT\_IN-} = V_{CM} - \frac{1}{2}V_{REF}.$$  $$V_{REF}$$ is as described above.

$V_{REF\_OUT\_MID}$ is the reference output mid-point and is derived from and equal to $V_{CM}$, $V_{REF\_OUT\_IN+}$, $V_{REF\_OUT\_IN-}$ and $V_{REF\_OUT\_MID}$ are brought out only to be by passed. Bypass this pin with 0.1µF capacitor to ground. Do not load these pins.

It is very important that all grounds associated with the reference voltage make connection to the ground plane at a single, quiet point to minimize the effects of noise currents in the ground path.

1.3 Signal Inputs

The signal inputs are $V_{IN+}$ and $V_{IN-}$. The signal input, $V_{IN}$, is defined as

$$V_{IN} = (V_{IN+}) - (V_{IN-}).$$

Figure 3 indicates the relationship between the input voltage and the reference voltages. Figure 4 shows the expected input signal range.

![FIGURE 3. Typical Input to Reference Relationship.](image)

![FIGURE 4. Expected Input Signal Range.](image)
Applications Information (Continued)

The ADC16061 performs best with a balanced input centered around $V_{CM}$. The peak-to-peak voltage swing at either $V_{IN+}$ or $V_{IN-}$ should be less than the reference voltage and each signal input pin should be centered on the $V_{CM}$ voltage. The two $V_{CM}$-centered input signals should be equal $180^\circ$ out of phase from each other. As a simple check to ensure this, be certain that the average voltage at the ADC input pins is equal to $V_{CM}$. Drive the analog inputs with a source impedance less than 100 Ohms.

The sign bit of the output word will be a logic low when $V_{IN+}$ is greater than $V_{IN-}$. When $V_{IN+}$ is less than $V_{IN-}$, the sign bit of the output word will be a logic high.

For single ended operation, one of the analog inputs should be connected to $V_{CM}$. However, SNR and SINAD are reduced by about 12dB with a single ended input as compared with differential inputs.

An input voltage of $V_{IN} = (V_{IN+}) - (V_{IN-}) = 0$ will be interpreted as mid-scale and will thus be converted to $0000,0000,0000,0000$, plus any offset error.

The $V_{IN+}$ and the $V_{IN-}$ inputs of the ADC16061 consist of an analog switch followed by a switched-capacitor amplifier. The capacitance seen at the analog input pins changes with the clock level, appearing as 12 pF when the clock is low, and 28 pF when the clock is high. It is recommended that the ADC16061 be driven with a low impedance source of 100 Ohms or less.

A simple application circuit is shown in Figure 6 and Figure 7. Here the LMH6550 fully differential amplifier is used to provide a balanced input to the ADC16061. Note that better noise performance is achieved when $V_{REF}^{IN}$ voltage is forced with a well-bypassed resistive divider. The resulting offset and offset drift is minimal.

1.4 $V_{CM}$ Analog Inputs

The $V_{CM}$ input of the ADC16061 is internally biased to 40% of the $V_A$ supply with on-chip resistors, as shown in Figure 5. The $V_{CM}$ pin must be bypassed to prevent any power supply noise from modulating this voltage. Modulation of the $V_{CM}$ potential will result in the introduction of noise into the input signal. The advantage of simply bypassing $V_{CM}$ (without driving it) is the circuit simplicity. On the other hand, if the $V_a$ supply can vary for any reason, $V_{CM}$ will also vary at a rate and amplitude related to the RC filter created by the bypass capacitor and the internal divider resistors. However, performance of this approach will be adequate for many applications.

By forcing $V_{CM}$ to a fixed potential, you can avoid the problems mentioned above. One such approach is to buffer the 2.0 Volt reference voltage to drive the $V_{CM}$ input, holding it at a constant potential as shown in Figure 6 and Figure 8. If the reference voltage is different from the desired $V_{CM}$, that desired $V_{CM}$ voltage may be derived from the reference or from another stable source.

Note that the buffer used for this purpose should be a slow, low noise amplifier. The LMC660, LMC662, LMC272 and LMC7101 are good choices for driving the $V_{CM}$ pin of the ADC16061.

If it is desired to use a multiplexer at the analog input, that multiplexer should be switched at the rising edge of the clock signal.

2.0 DIGITAL INPUTS

Digital Inputs consist of CLOCK, RESET, CAL, RD and PD. All digital input pins should remain stable from the fall of the clock until 30ns after the fall of the clock to minimize digital noise corruption of the input signal on the die.

2.1 The CLOCK signal drives an internal phase delay loop to create timing for the ADC. Drive the clock input with a stable, low phase jitter clock signal in the range of 300 kHz to 2.5 MHz. The trace carrying the clock signal should be as short as possible. This trace should not cross any other signal line, analog or digital, not even at 90˚.

The CLOCK signal also drives the internal state machine. If the clock is interrupted, the data within the pipeline could become corrupted.

A 100 Ohm damping resistor should be placed in series with the CLOCK pin to prevent signal undershoot at that input.

2.2 The RESET input is level sensitive and must be pulsed high for at least two clock cycles to reset the ADC after power-up and before calibration (See Timing Diagram 2).

2.3 The CAL input is level sensitive and must be pulsed high for at least two clock cycles to begin ADC calibration (See Timing Diagram 2). Reset the ADC16061 before calibrating. Re-calibrate after the temperature has changed by more than 50˚C since the last calibration was performed and after return from power down.

During calibration, use the same clock frequency that will be used for conversions to avoid excessive offset errors.

Calibration takes 272,800 clock cycles. Irrelevant data may appear at the data outputs during RESET or CAL and for 13 clock cycles thereafter. Calibration should not be started until the reference outputs have settled (100ms with 1µF capacitors on these outputs) after power up or coming out of the power down mode.

2.4 RD pin is used to READ the conversion data. When the RD pin is low, the output buffers go into the active state. When the RD input is high, the output buffers are in the high impedance state.

2.5 The PD pin, when low, holds the ADC16061 in a power-down mode where power consumption is typically less than 2mW to conserve power when the converter is not being used. Power consumption during shut-down is not affected by the clock frequency, or by whether there is a clock signal present. The data in the pipeline is corrupted while in the power down mode. The ADC16061 should be reset and calibrated upon returning to normal operation after a power down.
Applications Information (Continued)

3.0 OUTPUTS
The ADC16061 has four analog outputs: \( V_{\text{REF}+ \text{ OUT}} \), \( V_{\text{REF}− \text{ OUT}} \), \( V_{\text{REF} \text{ M ID}} \), and \( V_{\text{CM}} \). There are 17 digital outputs: EOC (End of Conversion) and 16 Data Output pins.

3.1 The reference output voltages are made available only for the purpose of bypassing with capacitors. These pins should not be loaded with more than 10 \( \mu \text{A} \) DC. These output voltages are described in Section 1.3.

3.2 The EOC output goes low to indicate the presence of valid data at the output data lines. Valid data is present the entire time that this signal is low, except during reset. Corrupt or irrelevant data may appear at the data outputs when the RESET pin or the CAL pin is high.

3.3 The Data Outputs are TTL/CMOS compatible. The output data format is two’s complement. Valid data is present at these outputs while the EOC pin is low. While the \( t_{\text{EOC}} \) time and the \( t_{\text{DATA VALID}} \) time provide information about output timing, a simple way to capture a valid output is to latch the data on the rising edge of the CCLK (pin 10).

Also helpful in minimizing noise due to output switching is to minimize the load currents at the digital outputs. This can be done by connecting buffers between the ADC outputs and any other circuitry. Only one input should be connected to each output pin. Additionally, inserting series resistors of 47 or 56 Ohms at the digital outputs, close to the ADC pins, will isolate the outputs from other circuitry and limit output currents. (See Figure 6).

4.0 POWER SUPPLY CONSIDERATIONS
Each power supply pin should be bypassed with a parallel combination of a 10 \( \mu \text{F} \) capacitor and a 0.1 \( \mu \text{F} \) ceramic chip capacitor. The chip capacitors should be within 1/2 centimeter of the power pins. Leadless chip capacitors are preferred because they provide low lead inductance.

While a single 5V source is used for the analog and digital supplies of the ADC16061, these supply pins should be well isolated from each other to prevent any digital noise from being coupled to the analog power pins. Supply isolation with ferrite beads is shown in Figure 6 and Figure 8.

As is the case with all high-speed converters, the ADC16061 is sensitive to power supply noise. Accordingly, the noise on the analog supply pin should be kept below 15 mVp-p.

No pin should ever have a voltage on it that is in excess of the supply voltages, not even during power up or power down.

The \( V_{\text{o}} \) I/O provides power for the output drivers and may be operated from a supply in the range of 2.7V to the \( V_{\text{o}} \) supply (nominal 5V). This can simplify interfacing to 3.0 Volt devices and systems. Powering \( V_{\text{o}} \) I/O from 3 Volts will also reduce power consumption and noise generation due to output switching. DO NOT operate the \( V_{\text{o}} \) I/O at a voltage higher than \( V_{\text{o}} \) or \( V_{\text{A}} \).

![Figure 6. Simple application circuit with single-ended to differential buffer.](image-url)
5.0 LAYOUT AND GROUNDING

Proper routing of all signals and proper ground techniques are essential to ensure accurate conversion. Separate analog and digital ground planes may be used if adequate care is taken with signal routing, but may result in EMI/RFI. A single ground plane with proper component placement with yield good results while minimizing EMI/RFI.

Analog and digital ground current paths should not coincide with each other as the common impedance will cause digital noise to be added to analog signals. Accordingly, traces carrying digital signals should be kept as far away from traces carrying analog signals as possible. Power should be routed with traces rather than the use of a power plane. The analog and digital power traces should be kept well away from each other. All power to the ADC16061 should be considered analog. The DGND I/O pin should be considered a digital ground and not be connected to the ground plane in close proximity with the other ground pins of the ADC16061.

The ground return for the digital supply (DGND I/O) carries the ground current for the output drivers and is isolated on the die from the other ground pins. The DGND I/O current can exhibit high transients that could add noise to the conversion process. To prevent this from happening, the DGND I/O current should NOT be connected in close proximity to any of the ADC16061’s other ground pins.

Capacitive coupling between the typically noisy digital ground plane and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and

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**FIGURE 7.** Differential drive circuit of Figure 6. Lower offset can be realized by using 0.1% resistors in place of the 1% resistors.

**FIGURE 8.** Driving the signal inputs with a transformer.
Applications Information  (Continued)

remedy. The solution is to keep the analog circuitry separated from the digital circuitry and from the digital ground plane.

Digital circuits create substantial supply and ground current transients. The logic noise thus generated could have significant impact upon system noise performance. The best logic family to use in systems with A/D converters is one which employs non-saturating transistor designs, or has low noise characteristics, such as the 74LS, 74HC(T) and 74AC(T)Q families. The worst noise generators are logic families that draw the largest supply current transients during clock or signal edges, like the 74F and the 74AC(T) families.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

Each bypass capacitor should be located as close to the appropriate converter pin as possible and connected to the pin and the appropriate ground plane with short traces. The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter’s input and ground should be connected to a very clean point in the ground return.

Generally, analog and digital lines should cross each other at 90 degrees to avoid getting digital noise into the analog path. To maximize accuracy in high speed, high resolution systems, however, avoid crossing analog and digital lines altogether. It is important to keep any clock lines isolated from ALL other lines, including other digital lines. Even the generally accepted 90 degree crossing should be avoided as even a little coupling can cause problems at high frequencies. This is because other lines can introduce phase noise (jitter) into the clock line, which can lead to degradation of SNR.

Best performance at high frequencies and at high resolution is obtained with a straight signal path. That is, the signal path through all components should form a straight line wherever possible.

Be especially careful with the layout of inductors. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors should not be placed side by side, not even with just a small part of their bodies beside each other.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter’s input and ground should be connected to a very clean point in the ground plane. We recommend the use of a single ground plane. That is, do not split the analog and digital ground planes. Rather, use a split power plane.

Figure 9 gives an example of a suitable layout. All analog circuitry (input amplifiers, filters, reference components, etc.) and interconnections should be placed in an area reserved for analog circuitry. All digital circuitry and I/O lines should be placed in an area reserved for digital circuitry. Violating these rules can result in digital noise getting into the analog circuitry, which will degrade accuracy and dynamic performance (THD, SNR, SINAD).

All ground connections should have a low inductance path to ground.
6.0 DYNAMIC PERFORMANCE
To achieve the best dynamic performance with the ADC16061, the clock source driving the CLK input must be free of jitter. For best a.c. performance, isolate the ADC clock from any digital circuitry with buffers, as with the clock tree shown in Figure 10.

As mentioned in section 5.0, it is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce phase noise (jitter) into the clock signal, which can lead to increased distortion. Even lines with 90° crossings have capacitive coupling, so try to avoid even these 90° crossings of the clock line.

7.0 COMMON APPLICATION PITFALLS
Driving the inputs (analog or digital) beyond the power supply rails. For proper operation, all inputs should not go more than 100 mV beyond the supply rails (more than 100 mV below the ground pins or 100 mV above the supply pins). Exceeding these limits on even a transient basis may cause
Applications Information  (Continued)

faulty or erratic operation. It is not uncommon for high speed digital circuits (e.g., 74F and 74AC devices) to exhibit under-shoot that goes more than a volt below ground. A resistor of about 50 to 100 Ω in series with the offending digital input will eliminate the problem.

Do not allow input voltages to exceed the supply voltage during power up.

Be careful not to overdrive the inputs of the ADC16061 with a device that is powered from supplies outside the range of the ADC16061 supply. Such practice may lead to conversion inaccuracies and even to device damage.

**Attempting to drive a high capacitance digital data bus.** The more capacitance the output drivers must charge for each conversion, the more instantaneous digital current flows through VD I/O and DGND I/O. These large charging current spikes can couple into the analog circuitry of the ADC16061, degrading dynamic performance. Adequate bypassing and maintaining separate analog and digital ground planes will reduce this problem. The digital data outputs should be buffered (with 74ACQ541, for example). Dynamic performance can also be improved by adding series resistors at each digital output, close to the ADC16061, which reduces the energy coupled back into the converter output pins by limiting the output current. A reasonable value for these resistors is 100 Ω.

**Using an inadequate amplifier to drive the analog input.** As explained in Section 1.3, the capacitance seen at the input alternates between 12 pF and 28 pF, depending upon the phase of the clock. This dynamic load is more difficult to drive than is a fixed capacitance.

If the amplifier exhibits overshoot, ringing, or any evidence of instability, even at a very low level, it will degrade performance. Amplifiers that have been used successfully to drive the analog inputs of the ADC16061 include the LMH6550, LM6152, LM6154, LM6181 and the LM6182. A small series resistor at each amplifier output and a capacitor across the analog inputs (as shown in Figure 7) will improve performance.

**Operating with the reference pins outside of the specified range.** As mentioned in section 1.2, \( V_{REF} \) should be in the range of

\[
1.8V \leq V_{REF} \leq 2.2V
\]

with \( V_{REF+} \leq 1.0V \). Operating outside of these limits could lead to excessive distortion or noise.

**Using a clock source with excessive jitter, using an excessively long clock signal trace, or having other signals coupled to the clock signal trace.** This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance.

**Connecting pins marked “NC” to any potential.** Some of these pins are used for factory testing. They should all be left floating. Connecting them to ground, power supply, or some other voltage could result in a non-functional device.
Physical Dimensions  inches (millimeters)
unless otherwise noted

52-Lead Thin Quad Flat Pack
Ordering Number ADC16061CCVT
NS Package Number VEG52A

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

BANNED SUBSTANCE COMPLIANCE
National Semiconductor follows the provisions of the Product Stewardship Guide for Customers (CSP-9-111C2) and Banned Substances and Materials of Interest Specification (CSP-9-111S2) for regulatory environmental compliance. Details may be found at: www.national.com/quality/green.

Lead free products are RoHS compliant.

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